Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 1. Please add new claims 32-49, as follows:

Listing of Claims:

1-31. (Cancelled)

32. (New) A method for accessing a memory array, comprising:

reading data and an associated error correction code from a location in the memory array;

storing the data in a memory;

modifying at least a portion of the data; and

when writing the modified data to the memory array,

updating the data stored in the memory with the modified portion of the data;

calculating a new error correction code based on the updated data in the memory; and

storing the updated data and the new error correction code to the location in the memory array.

33. (New) The method of claim 32 wherein modifying at least a portion of the data comprises performing graphics processing operations on the data.

34. (New) The method of claim 32 wherein updating comprises logically combining the stored data and the modified data together.

35. (New) The method of claim 32 wherein updating the data stored in the memory with the modified portion of the data comprises:

determining whether a write address corresponds to an address of data previously stored in the memory;

accessing the data stored in the memory based on the write address if correspondence is determined; and

logically combining the stored data and the modified data together and storing the modified data in the memory location in the memory where the data was previously stored.

36. (New) The method of claim 32, further comprising:

substantially concurrent with the reading and storing of data, updating second data previously stored in a second memory with a modified portion of the second data; and

substantially concurrent with the updating of the data, reading third data and storing the third data in the second memory.

37. (New) The method of claim 32 wherein the memory array is an embedded memory.

38. (New) The method of claim 32, further comprising providing the data read from the location to an output bus for provision to a requesting entity.

39. (New) A method for accessing a memory array, comprising:

reading first data and an associated error correction code from a first location in the memory array;

storing the first data in a first memory;

substantially concurrent with the reading and storing of the first data,

updating second data previously stored in a second memory with modified data;

calculating a new error correction code based on the updated second data in the second memory; and

storing the updated second data and the new error correction code to the location in the memory array from which the original second was read;

modifying at least a portion of the first data;

reading new data from a new location in the memory array;

storing the new data in the second memory; and

substantially concurrent with the reading and storing of the new data,

updating the first data stored in a first memory with the modified portion of the first data;

calculating a new error correction code based on the updated first data in the first memory; and

storing the updated first data and the new error correction code to the first location in the memory array.

40. (New) The method of claim 39 wherein modifying at least a portion of the first data comprises performing graphics processing operations on the first data.

41. (New) The method of claim 39 wherein updating the first and second data comprises logically combining the stored data and the modified data together.

42. (New) The method of claim 39 wherein updating the first and second data stored in the memory with the modified portion of the data comprises:

determining whether a write address corresponds to an address of data previously stored in the memory;

accessing the data stored in the memory based on the write address if correspondence is determined; and

logically combining the stored data and the modified data together and storing the modified data in the memory location in the memory where the data was previously stored.

43. (New) The method of claim 39 wherein the memory array is an embedded memory.

44. (New) The method of claim 39, further comprising providing the first data to an output bus for provision to a requesting entity.

45. (New) A memory system, comprising:

an embedded memory having a read data port and a write data port;

an error-correction code (ECC) generator coupled to the write data port and configured to generate an associated ECC for data written to the embedded memory;

an ECC check circuit coupled to the read data port and configured to confirm the integrity of the data based on the associated ECC;

a memory having an output coupled to the ECC generator and further having an input coupled to the ECC check circuit, the memory configured to store data read from the embedded memory and to store a memory address associated with the stored data, the memory further configured to output the stored data associated with a memory address in response to receiving the same;

a first selection circuit having an input coupled to the output of the first memory, and a first output coupled to a read bus and a second output coupled to the ECC generator and the write data port;

a second selection circuit having an output, and further having a first input coupled to the ECC check circuit and a second input coupled to a write bus;

combination logic having an output coupled to the input of the memory, a first input coupled to the output of the memory and a second input coupled to the ECC check circuit, the combination logic configured to combine data applied to the first and second inputs and provide combined data at the output; and

a control circuit coupled to the first and second selection circuits, the memory, and the combination logic, the control circuit configured to control the first and second selection circuits and coordinate the storing of data from the embedded memory in the memory and

provide the data to the output bus, and in response to receiving a write request, coordinate the combining of modified data received from the write bus with corresponding original data previously stored in the memory and further provide the combined data for ECC calculation and writing to the memory location in the embedded memory from where the original data was read.

46. (New) The apparatus of claim 45, further comprising:

a second memory an output coupled to the ECC generator and an input coupled to the ECC check circuit, the second memory configured to store data read from the embedded memory and to store a memory address associated with the stored data, the memory further configured to output the stored data associated with a memory address in response to receiving the same;

second combination logic having an output coupled to the second memory, a first input coupled to the output of the second memory, and a second input coupled to the ECC check circuit, the second combination logic configured to combine data applied to the first and second inputs and provide combined data at the output.

47. (New) The apparatus of claim 46 wherein the control circuit is further configured to coordinate the storing of data from the embedded memory in the second memory and provide the data to the output bus, and in response to receiving a write request, coordinate the combining of modified data received from the write bus with corresponding original data previously stored in the second memory and further provide the combined data for ECC calculation and writing to the memory location in the embedded memory from where the original data was read.

48. (New) The apparatus of claim 45 wherein the memory comprises a static random access memory.

49. (New) The apparatus of claim 45 wherein the embedded memory comprises a dual-port embedded memory.